Restriction

As claim 2 is generic to claims 3, 4, 6, 7, and 9, Applicant request examination of claims 4, 6, 7, and 9 upon the allowance of independent claim 2. *See* 37 C.F.R. § 1.141; MPEP §§ 806.04(d) and 809.02.

Drawings

The drawings are objected to because reference number 9 is allegedly not included. This objection is traversed, and reconsideration and withdrawal thereof requested.

Reference number 9, is described as an under-fill resin on page 7, line 29 of the instant specification. Reference number 9 is shown in the following Figures: 2, 3, 6, 7, 9, 11 and 12.

Claim Rejections Under 35 U.S.C. § 112

Claims 2 and 3 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite because the phrase "the same" in claim 2 allegedly lacks antecedent basis. This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested.

Applicant believes that claim 2, as originally presented, is definite. However, in order to advance prosecution, claim 2 has been amended to address the asserted informality. Applicant submits that claims 2 and 3 fully comport with the requirements of 35 U.S.C. § 112.

Claim Rejections Under 35 U.S.C. § 103

Claims 2 and 3 are rejected under 35 USC § 103(a) as being unpatentable over Bertin et al. (U.S. Patent No. 6,222,276). This rejection is traversed, and reconsideration and withdrawal thereof requested. The following is a comparison of the invention as claimed and the cited prior art.

An aspect of the invention, per claim 2, is a semiconductor device comprising a BGA substrate having one principal plane furnished with a large number of solder balls. The solder balls constitute a ball grid array. The semiconductor device further comprises a first semiconductor chip including bumps and active regions. The bumps and active regions are formed on a first side of the semiconductor chip. The bumps serve as electrodes attached to the one principal plane of the BGA substrate. A first chip capacitor is attached to the active regions of the first semiconductor chip or to the opposite side of the active regions of the first semiconductor chip. The first chip capacitor reduces power source noise.

The instant semiconductor device minimizes inductance between the first chip capacitor and the first semiconductor chip, thereby reducing power source noise. With this structure a small number of capacitor chips provide sufficient power source noise reduction.

The Examiner asserts that Bertin substantially teaches the claimed semiconductor device except for the BGA. However, the Examiner considers it to be obvious to form a BGA on the surface of the structure of Bertin because BGA are widely known/used connection means.

Contrary to the Examiner's assertion, Bertin does not teach or suggest the claimed semiconductor. The Examiner acknowledges that Bertin does not disclose a BGA connected to the substrate, as required by claim 2. The Examiner's rationale for including a BGA in the device of Bertin is not supported by the disclosure of Bertin. Rather, Bertin teaches away from including a BGA connected to the substrate.

A prior art reference must be considered in its entirety, i.e., as a <u>whole</u>, including portions that would lead away from the claimed invention. Such a teaching away from a

claimed invention constitutes potent evidence of non-obviousness. See, for example, ***In re Bell***, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); ***In re Hedges***, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); ***W.L. Gore & Assoc., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Bertin teaches away from including a BGA in its semiconductor device because Bertin expressly teaches,

> In the past, semiconductor packages have been electrically interconnected through wire bonding and/or the use of a C4 flip chip. Unfortunately, as packages become more dense and total performance gain becomes more important for high power chips in the system, the use of . . . flip chips to form off-chip connections is not practical in many applications . . . . the thermal properties of the flip chip severely limit the ability to cool high power chips, and adding an external heat sink to provide thermal conduction causes packaging constraint and increased chip operation ambient temperature.

(column 1, lines 21-34). BGA connections are made via the flip chip bonding method. In view of the express teaching of Bertin of thermal management problems of flip chips, one of ordinary skill in the art would **not** be motivated to modify the teaching of Bertin to attach the semiconductor chip via a BGA to the substrate.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Fine*, 835 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988);

In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). There is no teaching, suggestion, or motivation to modify the semiconductor device of Bertin to include a BGA substrate wherein the semiconductor chip is attached to the principal plane of the BGA substrate, as required by claim 2.

Although a reference can be modified, the prior art must suggest the desirability of modifying a reference. *See In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). The Examiner's conclusion that it would have been obvious to modify the structure of Bertin in order to provide inexpensive and compacted connection means is not supported by Bertin. Bertin, contrary to the Examiner's assertion, teaches against using a BGA substrate.

In rejecting a claim under 35 U.S.C. § 103, the Examiner is required to discharge the initial burden by, *inter alia*, making **"clear and particular"** factual findings as to a **specific understanding** or **specific technological principle** which would have **realistically** impelled one having ordinary skill in the art to modify an applied reference to arrive at the claimed invention based upon facts, -- not generalizations. *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 57 USPQ2d 1161 (Fed. Cir. 2000); *Ecolochem Inc. v. Southern California Edison, Co.*, 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Kotzab*, 217 F.3d 1365, 55 USPQ2d 1313 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). That burden has not been discharged, as the Examiner has provided not provide a factual basis for modifying Bertin's semiconductor device to provide the claimed device.

The Examiner did not make the requisite "clear and particular" factual findings to support the conclusion that one having ordinary skill in the art would have been realistically lead one to deviate from the Bertin methodology of forming a semiconductor

device. Instead, the Examiner merely announced that because BGA are a widely known/used connection means it would have been obvious to modify the teaching of Bertin.

There is no factual basis in the cited prior art to support the conclusion that one having ordinary skill in the art would have been led to form a semiconductor device with a BGA substrate having a principal plane furnished with a large number of solder balls and a first semiconductor chip including bumps and active regions formed on a first side of the semiconductor chip attached to the principal plane of the BGA substrate, and a first chip capacitor attached to the semiconductor chip. The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). The Examiner has not met the burden of identifying a source in the applied prior art for the required realistic motivation because Bertin does not suggest a semiconductor device comprising a BGA substrate having one principal plane furnished with a of solder ball grid array, a first semiconductor chip including bumps and active regions formed on a first side of the semiconductor chip, wherein the bumps are attached to one principal plane of the BGA

substrate, and a first chip capacitor attached to the first semiconductor chip, as required by claim 2. Rather, Bertin teaches away from using BGA substrate.

The only teaching of a semiconductor device comprising a BGA substrate having one principal plane furnished with a solder ball grid array, a first semiconductor chip including bumps and active regions formed on a first side of the semiconductor chip, wherein the bumps are attached to the one principal plane of the BGA substrate, and a first chip capacitor attached to the first semiconductor chip is found in Applicant's disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner's conclusion of obviousness is not supported by any factual evidence. The Examiner's retrospective assessment of the claimed invention and use of unsupported conclusory statements are not legally sufficient to generate a case of *prima facie* obviousness. The motivation for modifying the prior art must come from the prior art and must be based on facts.

The dependent claims further distinguish the claimed semiconductor device. For example, claim 3 requires that the first semiconductor chip includes through-type via contacts extending from the active regions to the opposite side in the first semiconductor chip, and the first chip capacitor is electrically connected to the active regions through the through-type via contacts. The claimed semiconductor device with these additional limitations is not suggested by cited prior art.

In light of the Amendments and Remarks above, this application is in condition for allowance and the case should be passed to issue. If there are any questions regarding this

Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. This attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at line 23 of page 2 has been amended as follows:

The BGA type semiconductor device is [the to be] at its limit of fabrication when coming to measure about 40 mm per side. When large-sized devices carry numerous terminals, they may adopt a pin grid array structure. The pin grid array structure, however, requires installing a socket between the semiconductor chip and the mounting substrate, which raises fabrication costs.

IN THE CLAIMS:

Claim 2 had been amended as follows:

2. (Amended) A semiconductor device comprising:

a BGA substrate having one principal plane furnished with a large number of solder balls, said solder balls constituting a ball grid array;

a first semiconductor chip including bumps and active regions [formed on the same side as said bumps] , said bumps and active regions formed on a first side of the semiconductor chip, said bumps serving as electrodes attached to said one principal plane of said BGA substrate; and

a first chip capacitor attached to said active regions of said first semiconductor chip or to the opposite side of said active regions of said first semiconductor chip, said first chip capacitor serving to reduce power source noise.